Abstract of the Disclosure:

The invention relates to a memory circuit having a memory cell array. Memory cells in the memory cell array can be addressed via word lines and bit lines and can be written to via write amplifiers. Each of the write amplifiers is assigned to a plurality of bit lines. A datum can be written, in accordance with a write address, to a memory cell via the addressed bit line using the assigned write amplifier. An address decoding circuit is provided to simultaneously activate a plurality of the write amplifiers depending on a test mode signal so that the plurality of write amplifiers write the test datum present via the respectively assigned bit lines.

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